AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with a first layer and a second mark portion associated with a second layer, wherein each mark portion comprises a ~~single~~ two dimensional generally orthogonal array of individual test structures.

2. (Currently Amended) An overlay metrology mark in accordance with claim 1 wherein each mark portion is ~~developed~~ within or on the said layer.

3. (Currently Amended) An overlay metrology mark in accordance with claim 2 wherein each mark portion is ~~printed~~ formed on the said layer by a microlithographic process.

4. (Currently Amended) An overlay metrology mark in accordance with claims 1 ~~or 2~~ wherein each mark portion comprises a single two dimensional generally substantially square array of individual test structures with generally constant spacing between test structures throughout the array.

5. (Currently Amended) An overlay metrology mark in accordance with claims 1 ~~or 2~~ wherein the spacing between test structures in the array comprising the first mark portion and the spacing between test structures in the array comprising the second mark portion is equivalent.

6. (Currently Amended) An overlay metrology mark in accordance with claim 5 wherein each mark portion has a generally square ~~overall~~ outline.

7. (Currently Amended) An overlay metrology mark in accordance with claim~~s~~ 1 ~~or 2~~ wherein each test structure has a width of around 0.5 to 2 μm.

8. (Currently Amended) An overlay metrology mark in accordance with claim~~s~~ 1 ~~or 2~~ wherein spacing between test structures in the array is between one and four times a ~~structure~~ width~~s~~ of the test structures.

9. (Currently Amended) An overlay metrology mark in accordance with claim~~s~~ 1 ~~or 2~~ wherein ~~the~~ individual test structures ~~making up each~~ of an array ~~are~~ have substantially identically size~~s~~~~d~~ and shape~~s~~~~d~~ and ~~have~~ are generally square ~~geometry~~.

10. (Currently Amended) An overlay metrology mark in accordance with claim~~s~~ 1 ~~or 2~~ wherein ~~the~~ individual test structures comprise arrangements of design rule sized sub-structures.

11. (Currently Amended) An overlay metrology mark in accordance with claim 10 wherein the arrangements of design rule sized sub-structures are ~~selected from~~ at least one of parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures, circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

12. (Currently Amended) An overlay metrology mark in accordance with claim 10 wherein sub-structures ~~are of~~ have design rule dimensions.

13. (Currently Amended) An overlay metrology mark in accordance with claim~~s~~ 1 ~~or 2~~ wherein the arrays of test structures making up the first and second mark portions are

disposed such that the first portion overlays the second portion and that the test structures of second portion are arrayed within the gaps between the test structures of the first portion and visible therebetween.

14. (Currently Amended) An overlay metrology mark in accordance with claim 13 wherein ~~each~~ individual test structures in the second portion ~~is~~ are located at the diagonal centre of a square bounded at each corner by test structures of the first portion.

15. (Currently Amended) An overlay metrology mark in accordance with claims 1 ~~or 2~~ wherein the test structures making up the first and second mark portions are disposed such that the first portion is laterally spaced from the second portion in a spacing direction parallel to a horizontal or vertical direction of the square arrays such that a notional line in the spacing direction can be drawn about which each array exhibits mirror symmetry.

16. (Original) An overlay metrology mark in accordance with claim 15 wherein each mark portion comprises an identical pattern of test structures.

17. (Original) A method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of:

laying down a first mark portion in association with a first layer;

and laying down a second mark portion in association with a second layer;

wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures.

18. (Original) A method for determining the relative position between two or more layers of an integrated circuit structure comprises the steps of:

laying down a first mark portion in association with a first layer;

laying down a second mark portion in association with a second layer;

wherein each mark portion comprises a single two dimensional generally square array of generally evenly spaced individual test structures;

optically imaging the two mark portions;

collecting and digitizing the image;

numerically analysing the digitized data to obtain a quantified measurement of the misalignment of the first and second mark portions.

19. (Original) The method of claim 18 wherein optical imaging of the mark is carried out using bright field microscopy.

20. (Currently Amended) The method of ~~one of~~ claim~~s~~ 17 ~~to 19~~ wherein ~~each~~ individual mark portion~~s~~ are ~~is~~ developed within or on the ~~said~~ layer.

21. (Currently Amended) The method of one of claim~~s~~ 17 ~~to 19~~ wherein ~~each~~ individual mark portion~~s~~ are formed ~~is laid down~~ by a ~~rn~~microlithographic process.

22. (Cancelled)

23. (New) The method of claim 18 wherein individual mark portions are developed within or on the layer.

24. (New) The method of claim 18 wherein individual mark portions are formed by a microlithographic process.